

PART OF CPS FC200

TELETYPEWRITER CONTROLLER INTERFACE
AND TIMING CIRCUITS

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CHANNEL INTERFACE CIRCUITS
ELEMENT IDENTIFICATION

TERM. MOD.	FNCT.	TERM.	LOC.
010N	I	303	2A1
010P	I	203	2A0
011N	I	002	2A2
011P	I	101	2A1
EN0B0	I	207	2A2
EN0B0	I	307	2A2
10P11	I	306	2A2
10P10	I	103	2A5
10P10	I	209	2A2
10P10	I	208	2A1
000	I	302	2A2
310T0	I	102	2A4
080N	#	305	2G1
080P	#	206	2G2
081N	#	304	2G2
081P	#	205	2G2
100	#	201	2G0
10P11	#	003	2G5
10P0	#	202	2G0
10N	#	108	2G3
10P	#	005	2G3
11N	#	104	2G4
11P	#	004	2G4
0A0T0	#	301	2G1
310T0	#	308	2G0
2A0T0	#	300	2G0

SYMBOL

LINE INTERFACE CIRCUITS
ELEMENT IDENTIFICATION

TERM. MOD.	FNCT.	TERM.	LOC.
AL00	I	017	3A3
AL00	I	116	3A4
AL00	I	015	3A5
AL00	I	014	3A5
RA0	I	016	3A3
RA0	I	115	3A4
RC0	I	114	3A5
RD0	I	113	3A4
TPA0	I	210	3A6
TP0	I	213	3A7
TP0	I	109	3A0
TP00	I	110	3A0
FR01	#	214	3G3
FR01	#	215	3G4
ACT1	#	216	3G5
PR01	#	217	3G4
SALM01	#	009	3G3
SALM01	#	011	3G4
SALM01	#	115	3G5
SALM01	#	316	3G5
SA0	#	310	3G6
SD0	#	309	3G7
SC0	#	108	3G0
SD0	#	008	3G9
+3	P	000	3G0
+2A	P	013, 112	3G1
+2A	P	019, 118	3G2
-2A	P	218, 318	3G1
GR0	C	200, 319	3G1
GR0	C	000	3G1

LINE TIMING CIRCUITS
ELEMENT IDENTIFICATION

TERM. MOD.	FNCT.	TERM.	LOC.
LT10N1	#	204	2G7

RECORD OF CHANGES

DWG. ISS.	REV. FURN.	STD.	MFR. DISC.	SEE NOTE

SUPPORTING INFORMATION

CATEGORY	NO.
CIRCUIT PACK CODE CONNECTOR ON FRAME	FC200 972A OR 972C
ACCEPTABLE SERIES	7

NOTES:

- GROUND RETURN.
- UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS.
CAPACITANCE VALUES ARE IN MICROFARADS.
VALUES PRECEDED BY THE SYMBOL + (PLUS)
OR - (MINUS) ARE IN VOLTS.
- BATTERY AND GROUND TERMINALS FOR INTEGRATED CIRCUITS.

IC CODE	BAT. TERM.	GRD. TERM.
155A	14	1
41N	3, 6, 7, 8	1, 2
41NE	14	2, 8
41DL	14	8

- BATTERY AND GROUND TERMINALS FOR THIS CIRCUIT PACK ARE AS FOLLOWS:

FUNCTION	TERMINAL
-2A	218, 318
+3	000
+2A	019, 118
+2AF	013, 112
GR0	200, 319, 000

- HORIZONTAL MOUNTING CENTERS AT 0.5 INCH.

SYSTEM USED ON	DESIGN CONTROL
COMMON SYSTEMS	1H

CURRENT DRAIN.

+2V	300mA
+24V	150mA
-24V	50mA

NOTICE - NOT FOR USE OR DISCLOSURE OUTSIDE THE BELL SYSTEM EXCEPT UNDER WRITTEN AGREEMENT.

3A

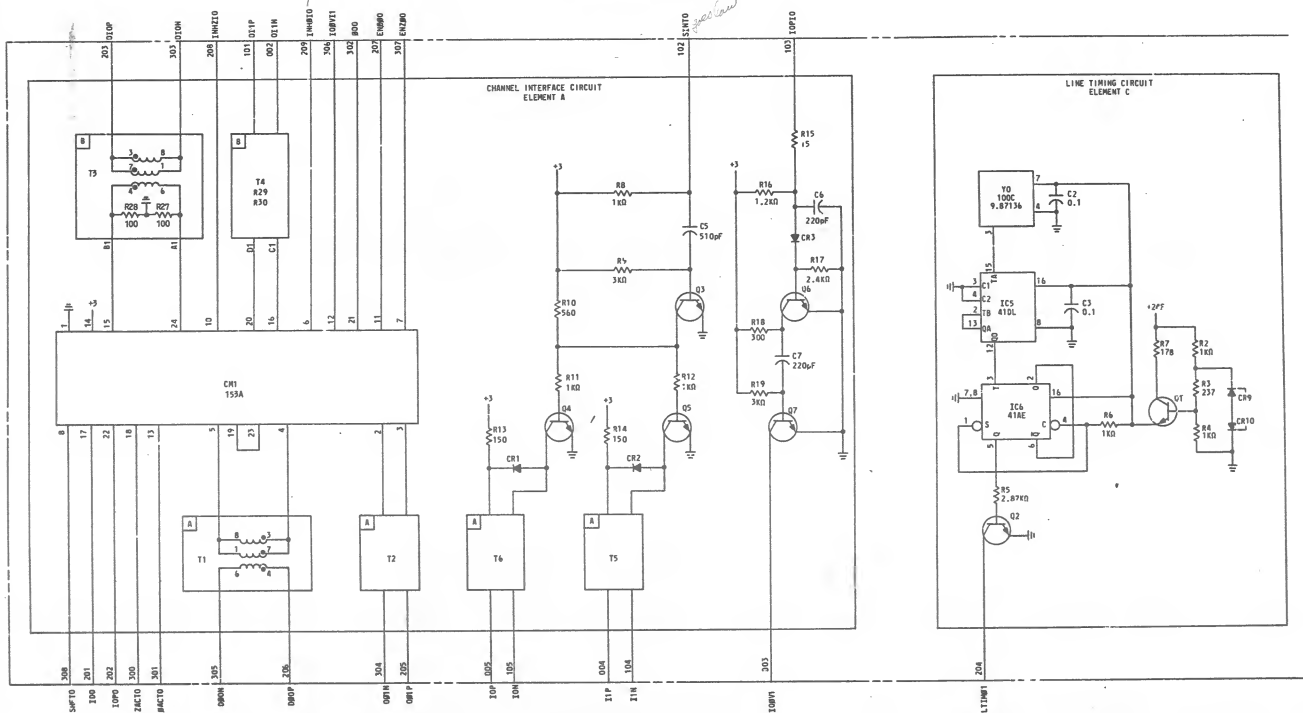
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FC200 CIRCUIT PACK

TELETYPEWRITER CONTROLLER
INTERFACE AND TIMING
CIRCUITSBELL TELEPHONE LABORATORIES
INCORPORATEDAT&T
STANDARDCPS-FC200
7 SHEETS

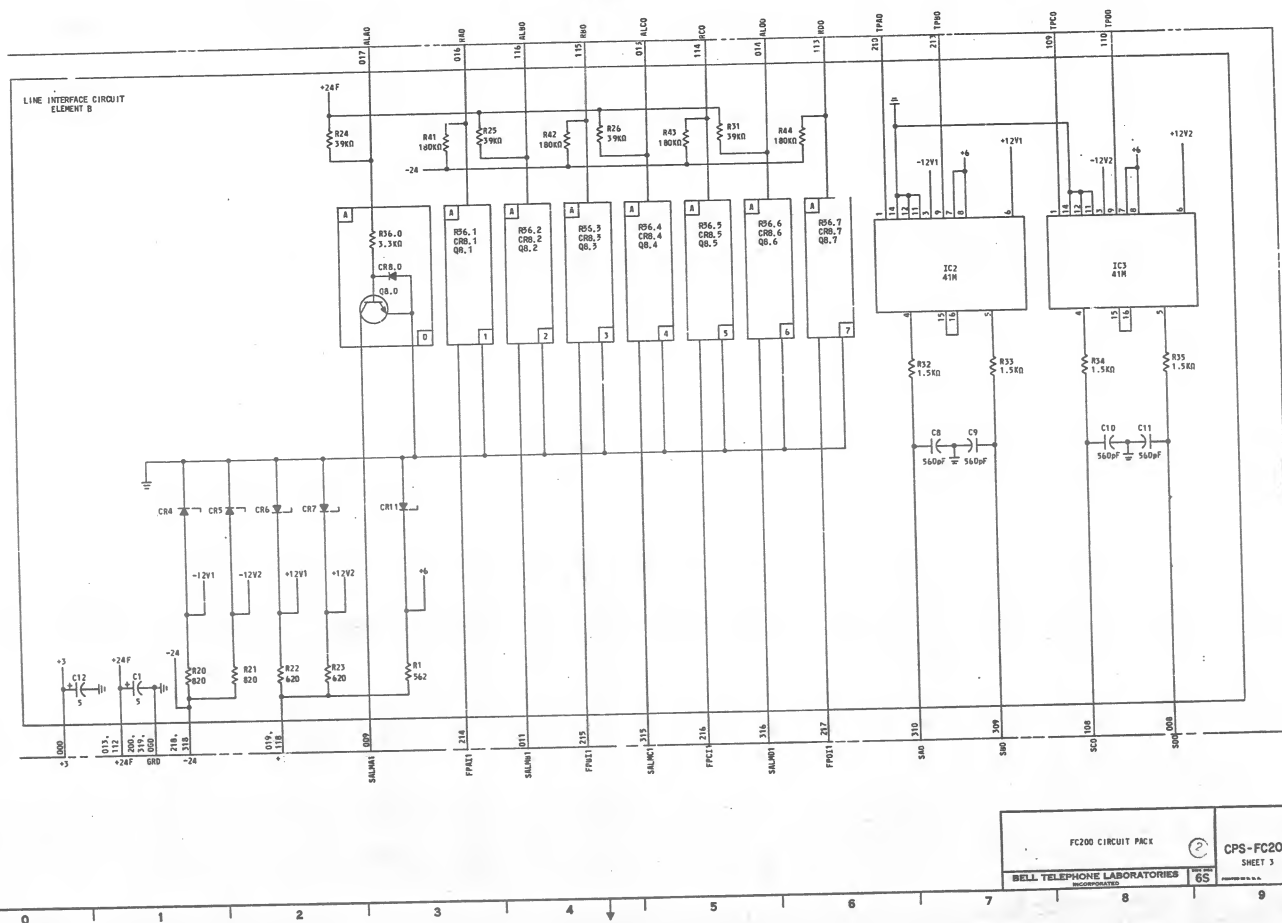
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PART OF CPS FC200
TELETYPEWRITER CONTROLLER INTERFACE AND
TIMING CIRCUITS



CPS-FC200

PART OF CPS FC200 TELETYPEWRITER CONTROLLER INTERFACE AND TIMING CIRCUITS



CPS-FC200

TELETYPEWRITER CONTROLLER INTERFACE AND
TIMING CIRCUITSTELETYPEWRITER CONTROLLER INTERFACE AND
TIMING CIRCUITS

RESISTOR (CONT)

CAPACITOR

DESIG	CODE
C1	601A, S
[2] C2, C3	KS-1977A L5, 0.1
C5	KS-1977A L1, 510p
C6	KS-1977A L1, 220p
C7	KS-1977A L1, 220p
C8	KS-1977A L1, 560p
C9	KS-1977A L1, 560p
C10	KS-1977A L1, 560p
C11	KS-1977A L1, 560p
C12	601A, S

CIRCUIT MODULE

<u>DESIG</u>	<u>CODE</u>
CM1	153A

CRYSTAL

DESIG	CODE
Y-3	170C 9.87136 MHZ

DIODE

DESIG	CODE
CR1	A58C
CR2	458C
CR3	A58C
CR4	808J
CR5	808J
CR6	808J
CR7	808J
[8] CR8, D-CR8, 7	458C

INTEGRATED CIRCUIT

<u>DESIG</u>	<u>CODE</u>
IC2	41M
IC3	41M
IC5	41OL
IC6	41AZ

RESISTOR

<u>CS</u>	<u>SIG</u>	<u>CODE</u>
R1		KS-20289 L&C, 562
R2		KS-20810 L1A, 18D
R3		KS-20816 L1A, 18D, 277
R4		KS-20616 L1A, 18D
R5		KS-20616 L1A, 2.87K
R6		KS-20816 L1A, 18D
R7		KS-20289 L&A, 178
R8		KS-16445 L1, 18D
R9		KS-16445 L1, 38D
R10		KS-16445 L1, 56D
R11		KS-16445 L1, 18D
R12		KS-16445 L1, 18D
R13		KS-16445 L1, 150
R14		KS-16445 L1, 150
R15		KS-16445 L1, 150
R16		KS-16445 L1, 280K

DESIG	CODE
R17	KS-16-645 L1, 2.0E
R18	KS-16-645 L1, 3.0E
R19	KS-16-645 L1, 3.0E
R20	KS-19-150 L1, 820
R21	KS-19-150 L1, 820
R22	KS-19-150 L1, 6.2E
R23	KS-19-150 L1, 6.2E
R24	KS-16-645 L1, 39K0
R25	KS-16-645 L1, 39K0
R26	KS-16-645 L1, 39K0
R27	KS-16-645 L1, 100
R28	KS-16-645 L1, 100
R29	KS-16-645 L1, 100
R30	KS-16-645 L1, 100
R31	KS-16-645 L1, 39K0
R32	KS-16-645 L1, 1.5E0
R33	KS-16-645 L1, 1.5E0
R34	KS-16-645 L1, 1.5E0
R35	KS-16-645 L1, 1.5E0
R36	KS-16-645 L1, 3.5E0
R41	KS-16-645 L1, 1.00K0
R42	KS-16-645 L1, 1.00K0
R43	KS-16-645 L1, 1.00K0
R44	KS-16-645 L1, 1.00K0

TRANSFORMER

DESIG	CODE
T1	2664
T2	
T3	
T4	
T5	
T6	2664

TRANSISTOR

OES16	CODE
Q1	92A
Q2	66S
Q3	
Q4	
Q5	
Q6	
Q7	
[8] 08.0-08.7	66S

CIRCUIT DESCRIPTION

A. FUNCTION

CIRCUIT PACK (CP) FC200 IS USED IN THE TELETYPEWRITER CONTROLLER (TTYC) CIRCUIT TO INTERFACE THE TTYC LOGIC CIRCUITRY TO THE 3A CENTRAL CONTROL (3A CC) AND THE TELETYPEWRITER (TTY).

B. DETAILED DESCRIPTION

LEADS HAVING DESIGNATION THAT END IN D ARE LOW WHEN ACTIVE OR IN THE ONE STATE. LEADS HAVING DESIGNATION THAT END IN 1 ARE HIGH WHEN ACTIVE OR IN THE ONE STATE.

CHANNEL INTERFACE CIRCUIT - ELEMENT 2

DATA IS PASSED BETWEEN THE 3A CC₁ TO THE TTYC IN SERIAL BIPOLAR DATA. A CARRYING LINE FROM THE 3A CC₂ IS TERMINATING IN THE TRANSFORMERS T3 AND TA AND THEIR ASSOCIATED RESISTORS. A CIRCUIT MODULE (C1) CONVERTS THE BIPOLAR INPUT DATA TO LOGIC-LEVEL SIGNALS, APPEARING ON LEAD IZD. A TIMING SIGNAL IS ALSO GENERATED BY C1 ON LEAD SHD SO THAT THE TTYC LOGIC CIRCUITS WILL SAMPLE THE DATA WHEN IT IS GIVEN IT. (FOR THE DESCRIPTION ON 153A VU, SEE THE RELATIONSHIP BETWEEN THE BIPOLAR INPUT AND LOGIC LEVEL DATA AND DATA LEADS.) THE DATA INPUT FROM CCO OR CCI? IS BLOCKED WHEN LEADS IZMDI OR IZMDI ARE ACTIVE. LEADS ZACTO OR BACTO ARE ACTIVE WHEN DATA IS BEING RECEIVED FROM CCO OR CCI?. THESE LEADS ARE ACTIVE WHEN CCO OR CCI? ARE ACTIVE. LEADS ZACTI (IE, ZACTO CONNECTED TO IZMDI AND BACTO CONNECTED TO IZMDI) TO LOCK OUT ONE CCI WHILE AN DATA IS BEING RECEIVED FROM THE OTHER.

IDPO IS ACTIVE WHILE INPUT DATA IS PRESENT. IT CAN BE CONNECTED TO IDPOH WHERE IT WILL TURN OFF Q6 AND ALLOW C7 TO CHARGE TO +3 VOLTS THROUGH R16. WHEN THE INPUT DATA STOPS, IDPO IS NO LONGER ACTIVE AND C6 CHARGES TO +3V THROUGH R16. WHEN IT REACHES APPROXIMATELY 1.5 VOLTS, Q6 WILL TURN ON AND DISCHARGE C7. Q7 WILL CUT OFF UNTIL C7 CAN CHARGE ITS VOLTAGE THROUGH R19 TO ABOUT 0.7 VOLTS IN THE OPPOSITE DIRECTION. THIS RESULTS IN A NOMINAL 450n PULSE ON LEAD IDPOV1. IDPOV1 IS CONNECTED TO IDPOV1T WHERE IT INITIALIZES CIRCUITS IN CMI. THIS SIGNAL CAN ALSO INITIALIZE OTHER TTY LOGIC CIRCUITS.

DATA IS SENT FROM THE TTTC TO THE 3A CC'S IN BIPOLAR FORM VIA COAXIAL CABLE CONNECTED TO 0B0P/N AND 0B1P/N. THE LOGIC - LEVEL SIGNAL OF DATA 'G' BE OUTPUTTED IS SET ON LEAD 0B0. TIMING FOR THE OUTPUT DATA IS DERIVED FROM AN ALL - ZERO'S INPUT DATA STREAM THAT IS SUPPLIED BY THE 3A CC DURING THE TIME WHEN THE TTTC IS EXPECTED TO OUTPUT DATA TO IT. LEADS EN20 AND ENB00 ENABLE THE OUTPUT DATA TO BE DIRECTED TO 3A C00, OR 3A C01.

LEAD SINTO IS ACTIVATED BY THE TTYC WHEN IT HAS COMPLETED A CHARACTER EXCHANGE WITH THE TTY. WHEN SINTO IS NOT ACTIVE, CS IS CHARGED TO ABOUT 10 VOLTS THROUGH R8. WHEN SINTO GOES ACTIVE, CS IS DISCHARGED AND CS VOLTS UNTIL C7 CAN CHANGE ITS CHARGE THROUGH R9. THIS RESULTS IN A NOISE BURST OUT OF C7. A 103 MHz SIGNAL IS SENT TO BOTH 3A CC'S VIA DRIVERS Q4 AND Q5 AND TRANSFORMERS T5 AND T6. THIS SIGNAL IS CONNECTED TO THE 3A CC INTERRUPT CIRCUITS WHEN THE 3A CC IS USED IN A SYSTEM THAT SERVICES ITS TTY'S ON A DEMAND BASIS.

LINE TIMING CIRCUIT - ELEMENT C

TO IS A CRYSTAL CONTROLLED OSCILLATOR WITH A FREQUENCY OF 9.87136MHZ. IC5 IS A 4-STAGE RIPLE COUNTER. IC6 IS A TOGGLE F/F. IC5 AND IC6 OVIIDE THE OSCILLATOR OUTPUT BY 32 TO PRODUCE A 308.48KHZ FREQUENCY (3.2A17USEC PERIOD) OUTPUT AT TERMINAL 204. Q2 INTERFACES THIS SIGNAL TO THE TTIC LOGIC WHERE IT IS USED TO DETERMINE BIT TIMING FOR THE CHARACTER EXCHANGE WITH THE TTY. Q1 IS A 5 VOLT REGULATOR TO SUPPLY TO, IC5

LINE INTERFACE CIRCUIT - ELEMENT 8

THIS CIRCUIT PROVIDES THE LEVEL CONVERSION FOR SIGNALS EXCHANGED BETWEEN THE TTYC AND THE TTY. THREE SIGNALS RECEIVED DATA, TRANSMITTED DATA, AND TTY ALARM ARE PROVIDED BY THE TTYC FOR EACH OF FOUR TTY PORTS. THE PORTS ARE Labeled A, B, C, AND D. THE LOGIC IN THIS CIRCUIT CONVERTS THE DATA SIGNALS TO RECEIVE - DATA SIGNALS FROM TTY PORTS TO THROUGH-O. THE DATA SIGNALS ARE ALSO USED TO MONITOR THE TTY ALARMS. IN THE OTHER DIRECTION, LOGIC SIGNALS TP80 THROUGH TP90 ARE SENT TO THE TTYC. THESE ARE CONNECTED TO EIA LEVEL ON LEADS SAO THROUGHTHROUGH SAI. THE TTYC IS RESPONSIBLE FOR DETECTING AND REPORTING TO THE ATN DEVICE, CMT J22, AND CMT J23, ANY TTY ALARM STATE BY R24, R25, R26, AND K31 TO PREVENT ERRONEOUS ACTIONS FROM UNEXPECTED TTY ALARMS. THE LOGIC IN THIS CIRCUIT ALSO MONITORS THE TTYC FOR DISCONNECTED PORT BY RAT THROUGH R44, R20 THROUGH R23, AND CRA THROUGH CR7 THROUGH CR11. PROPERLY TERMINATE THE TTYC BY THE ATNS. R32 THROUGH R35 AND CR12 THROUGH CR15.

C. SYMBOL/LEAD MNEMONIC

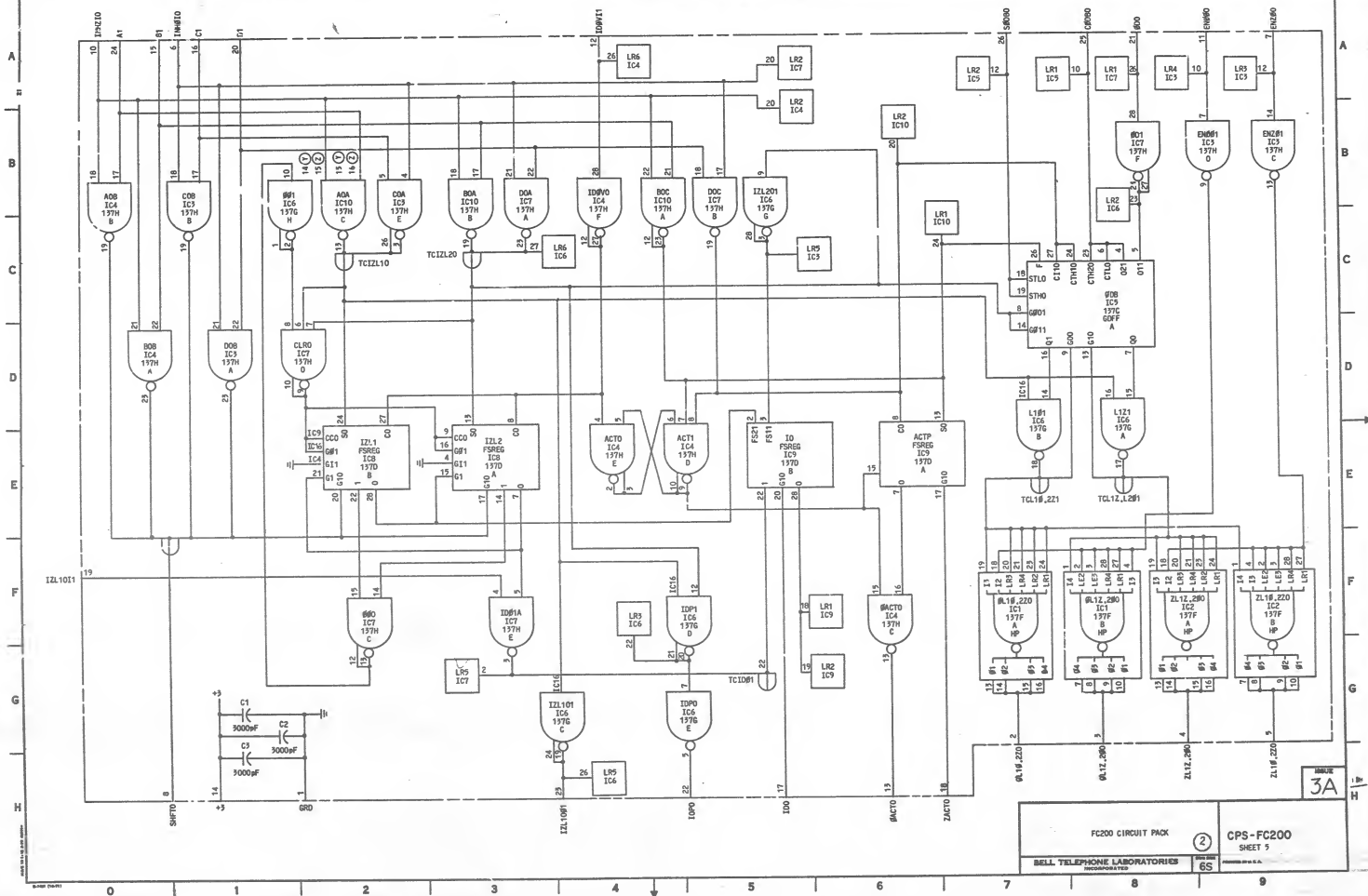
PHENONIC

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ALAG-00  EIA LEVEL, ALARM SIGNAL, FROM TTY PORTS A THROUGH D
CINOP-01 DATA INPUT FROM CCG NEGATIVE/POSITIVE
CINOP-02 INTERRUPT SIGNAL FROM CCG NEGATIVE/POSITIVE
CINOP-03 DATA OUTPUT TO CCG NEGATIVE/POSITIVE
CINOP-04 INTERRUPT SIGNAL FROM CCG NEGATIVE/POSITIVE
EMBO-00 ENABLE OUTPUT TO CCG NEGATIVE/POSITIVE
EMBO-01 LOGIC LEVEL, RECEIVED DATA SIGNAL, FROM TTY PORTS A
      THROUGH D
FPR1-011 INCOMING DATA OVER-INPUT
      INCOMING DATA OVER-OUTPUT
      INCOMING DATA PRESENT-INPUT
      INCOMING DATA PRESENT-OUTPUT
      INCOMING DATA
      INHIBIT INPUT FROM CCG
      INHIBIT OUTPUT TO CCG
      INTERRUPT SIGNAL TO CCG NEGATIVE/POSITIVE
      INTERRUPT SIGNAL FROM CCG NEGATIVE/POSITIVE
      LINE TYPING SIGNAL
      LINE TYPING SIGNAL
      LOGIC LEVEL, ACTIVE WITH THE TTYC
      OUTGOING DATA
      LOGIC LEVEL, RECEIVED DATA FROM TTY PORTS A THROUGH
      EIA LEVEL, ALARM SIGNAL, FROM TTY PORTS A THROUGH
      EIA LEVEL, TRANSMITTED DATA TO TTY PORTS A THROUGH
      SET INTERRUPT
      LOGIC LEVEL, TRANSMITTED DATA SIGNAL, TO TTY PORTS
      LOGIC LEVEL, ACTIVE WITH TTYC

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PART OF CMS 153A



PART OF CMS 153A

COMPONENT LIST INTEGRATED CIRCUIT

LOC CODE FLEM ID	IC1 157F (NOTE 1) DESIG SH LOC	IC2 157F (NOTE 1) DESIG SH LOC	IC3 157H DESIG SH LOC	IC4 157H DESIG SH LOC	IC5 157C DESIG SH LOC	IC6 157B DESIG SH LOC	IC7 157H DESIG SH LOC	IC8 157D DESIG SH LOC	IC9 157D DESIG SH LOC	IC10 157H DESIG SH LOC	LOC CODE ELEM ID
A	RL1F.220 SF7	2L12.200 SF8	D08 501	B08 530	908 568	L121 568	D08 580	12L2 563	ACTP 565	B0C 584	A
B	RL1F.200 SF8	2L10.220 SF9	C08 581	A08 580		L101 587	D0C 585	12L1 562	ID 565	B0A 583	B
C			EN201 589	RACTD 596		12L101 564	890 592			A0A 582	C
D			EN091 589	ACT1 564		10P1 594	CL00 501				D
E			C0A 582	ACT0 564		10P0 565	1001A 593				E
F			RACTD 595	10P0 584			901 588				F
G						12L201 585					G
H						991 581					H

CAPACITOR

DESIG	CODE
[3] C1-C3	B01A 3000pF

NOTES:

1. CAPACITOR CHIP B01A, 3000pF IS BONDED ON EACH SIDE OF 157F SIC.

RECORD OF CHANGES					
DWG	PREP	STD	APP	SEE	NOTE
155	PAUN				
3	Z	Y	Z		

SYMBOL	
1A	CH 153A
1B	1A1Z10
24	A1 SHFTD
15	01 12L1001
6	10H020
15	C1 100
20	01 RACTD
12	10H011
20	01 ZACTD
20	0000 RL12.200
25	0000 RL10.220
21	000 2L12.200
11	EN090 2L10.220
7	EN200

BATTERY AND GROUND TERMINALS FOR INTEGRATED CIRCUITS

IC CODE	BAT TERM	GRD TERM
157C	25	11
157D	25	11
157F	25, 26	11, 12
157G	25	11
157H	25	11

SUPPORTING INFORMATION

CATEGORY	NO
INTEGRATED CIRCUIT CODE	153A
ACCEPTABLE SERIES	3-4,4

FC200 CIRCUIT PACK

BELL TELEPHONE LABORATORIES

153A IC

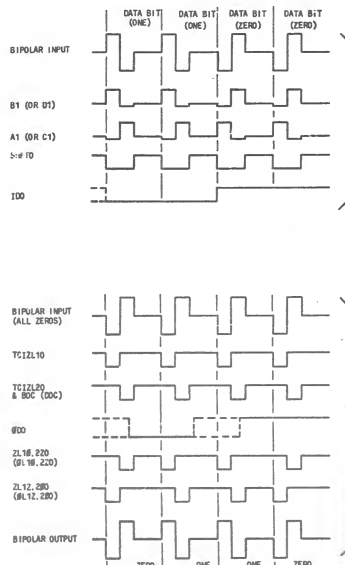
CPS-FC200

SHEET 6

3A

00523-8-84

TIMING DIAGRAM

FIG. 1
BIPOLAR TO LOGIC
LEVEL CONVERSION
USING CN 193AFIG. 2
LOGIC LEVEL TO
BIPOLAR CONVERSION
USING CN 193A

CIRCUIT DESCRIPTION

A. FUNCTION

CN 193A IS USED IN THE CONVERSION BETWEEN BIPOLAR SIGNALS ON THE 3A CC 1/2 DATA LINES AND LOGIC-LEVEL SIGNALS REQUIRED BY PERIPHERAL UNIT CONTROLLER CIRCUITS (SUCH AS THE TTY CONTROLLER).

B. DETAILED DESCRIPTION

LEADS HAVING DESIGNATIONS THAT END IN 1 ARE HIGH WHEN ACTIVE, OR IN THE ONE STATE. LEADS HAVING DESIGNATIONS THAT END IN 0 ARE LOW WHEN ACTIVE, OR IN THE ONE STATE. FLIP-FLOPS ARE SET TO THE ONE STATE AND CLEARED TO THE ZERO STATE.

BIPOLAR TO LOGIC LEVEL CONVERSION

THE CONTROLLER RECEIVED DATA LINE IS TRANSFORMER-COUPLED TO CN 193A ON LEADS A1 AND B1 FROM CCO, AND C1 AND D1 FROM CCI. THE DATA IS SORTED BY GATES A0A AND B0A AT TC1210, AND BY GATES B0A AND D0A AT TC1220. THE RELATIONSHIP BETWEEN THE BIPOLAR DATA, THE INPUT TO CN 193A, AND ITS LOGIC-LEVEL DATA (LOGIC) AND TIMING (SHIFT) OUTPUT SIGNALS, IS SHOWN IN FIG. 1. THE LOGIC POSITIVE AND NEGATIVE EXCURSIONS, A LOGICAL ZERO IS A NEGATIVE FOLLOWED BY A POSITIVE LOGIC. CLIPPING CIRCUITS, WHICH ARE PART OF GATES TO WHICH THE A1, B1, C1, AND D1 INPUTS CONNECT, LIMIT THE NEGATIVE EXCURSION AT THIS POINT, AND PREVENT RECOVERY PROBLEMS IN THESE GATES.

THE INPUT DATA LEAD (100) IS SET AT THE LEADING EDGE OF THE FIRST LOSE. THE TIMING SIGNAL IS THE TRAILING EDGE OF S-SHIFT WHICH OCCURS AT THE TRAILING EDGE OF THE SECOND LOSE. THUS, THE CONTROLLER IS SIGNALLED TO SAMPLE THE INCOMING DATA IN THE CENTER OF THE BIT PERIOD WHEN THE DATA LEAD IS STABLE. CARE HAS BEEN TAKEN TO MINIMIZE THE NUMBER OF GATES THAT CONTROL THE 100 AND S-SHIFT LEADS IN ORDER THAT VARIATIONS IN GATE DELAYS WILL NOT DESTROY THE RELATIONSHIP BETWEEN THESE SIGNALS. NOMINAL TIMES FOR THE 3A CC SERIAL 1/2 DATA ARE A 10-MS-BIT INTERVAL WITH 97.5-MS LOSES.

THE S-SHIFT LEAD IS CONTROLLED BY GATES A0B, B0B, C0B, AND D0B, AND FLIP-FLOPS 1211 AND 1212. INITIALLY, NONE OF THE GATES ARE ACTIVE AND BOTH FLIP-FLOPS ARE IN THE CLEARED STATE SO THAT S-SHIFT IS HIGH. IF B0B AND D0B ARE NOT ACTIVE, THE FIRST LOSE OF THE INPUT DATA BIT WILL ACTIVATE ONE OF GATES (DEPENDENT ON WHETHER THE BIT IS A ONE OR ZERO AND IF IT IS FROM CCO OR CCI) AND PULL S-SHIFT LOW. THE FIRST LOSE WILL ALSO ACTIVATE ONE OF THE GATES FORMING TC1210 OR TC1220 WHICH WILL SET ONE OF THE FLIP-FLOPS, 1211 OR 1212, DEPENDING ON CONDITIONS PREVIOUSLY DESCRIBED. THE PURPOSE OF THESE FLIP-FLOPS IS TO HOLD S-SHIFT LOW DURING ANY GAP THAT MIGHT BE PRESENT BETWEEN THE FIRST AND SECOND LOSES AND TO PREVENT THE SECOND LOSE FROM CHANGING THE STATE OF THE DATA FLIP-FLOP (10).

WHEN THE SECOND LOSE OF THE INCOMING DATA BIT IS ACTIVE THE STATE OF THE GATE ACTIVATED BY THE FIRST LOSE WILL BE ACTIVE AND IT WILL ALSO HOLD S-SHIFT LOW (A0B AND B0B ARE ONES AS ARE C0B AND D0B). THIS LOGIC WILL ALSO SET THE FLIP-FLOP (1211 OR 1212) THAT WAS NOT SET BY THE FIRST LOSE. WHEN THE SECOND FLIP-FLOP IS SET, IT INHIBITS THE PATH BY WHICH THE FIRST FLIP-FLOP WOULD SHIFT TO GROUND. WHEN THE FIRST LOSE IS OVER ONLY THE GATE ACTIVATED BY THE SECOND LOSE HOLDS S-SHIFT LOW.

WITH BOTH FLIP-FLOPS SET, THE INPUT TO C10D FROM B01 IS HIGH. THE OTHER INPUTS TO C10D, 100 AND 101, AND TC1210 ARE CONTROLLED BY THE DATA LOSES. WHEN THE FIRST LOSE IS GONE, ONLY THE SECOND LOSE CONTROLS C10D. WHEN THE SECOND LOSE EXPIRES, THE GATE HOLDING S-SHIFT IS DEASELED AND S-SHIFT WILL GO HIGH. C10D WILL GO LOW AT THIS TIME AND CLEAR BOTH FLIP-FLOPS. C10D LOW ALSO DISJUNCTIONS THE 1211 AND 1212 CONNECTION TO S-SHIFT SO THAT FALSE SIGNALS CANNOT OCCUR ON THIS LEAD AS THE FLIP-FLOPS CHANGE FROM THE 11 TO THE 00 STATE.

LEAD 100 IS CONTROLLED BY THE TO FLIP-FLOP. IT RETAINS THE LAST INCOMING DATA STATE UNTIL IT IS UPDATED BY THE FIRST LOSE OF A NEW DATA BIT. IF THE NEW DATA BIT IS A ZERO, TC1210 WILL BE ACTIVE FIRST AND DRIVE GATE 1210B HIGH. TERMINALS 19 AND 23 ARE EXTERNALLY TIED TOGETHER SO THAT 1210A HAS BOTH INPUTS HIGH. IT SHOULD BE NOTED THAT 1211 AND 1212 ARE INITIATED FROM THE CLEARED STATE AND THAT TC1210 SETS 1211 BUT DOES NOT AFFECT 1212. 1210A WILL PULL 1210B LOW, WHICH WILL CLEAR 10 AND DRIVE 100 HIGH, TO ITS ZERO STATE. WHEN THE SECOND LOSE IS ACTIVE FOR THE ZERO DATA BIT, TC1210 WILL DRIVE 1212 HIGH. HOWEVER, 1211 WILL BE SET BY THE FIRST LOSE, IN ORDER TO PREVENT 1210D FROM CHANGING THE 10 FLIP-FLOP.

IF THE INCOMING DATA BIT IS A ONE, TC1220 WILL BE ACTIVE FIRST. 1220B WILL BE HIGH WHILE 1211 IS CLEARED, AND THE TO FLIP-FLOP, 1220A, WILL BE SET. 100 WILL THEN BE LOW, WHICH IS THE ONE STATE. WHEN THE SECOND LOSE IS ACTIVE FOR THE INCOMING ONE, TC1210 IS ACTIVE, AND WILL DRIVE 1220B HIGH. TC1220, HOWEVER, WILL HAVE SET 1212, WHICH PREVENTS 1210A FROM CHANGING 10.

LEADS ZACTO AND BACTO INDICATE WHICH, IF ANY, CC IS ACTIVELY COMMUNICATING WITH THE CONTROLLER. THE ACT FLIP-FLOP, FORMED BY GATES ACTO AND ACT1, IS SET BY GATES B0C OR D0C TO INDICATE THAT ONE OF THE CC'S IS SUPPLYING INPUT DATA. FLIP-FLOP ACTP IS SET BY B0C WHEN CCI IS ACTIVE, AND IS CLEARED BY D0C WHEN CCI IS ACTIVE. THE ACT AND ACTP FLIP-FLOPS ARE COMBINED TO ACTIVE ZACTO WHEN CCI IS ACTIVE AND BACTO WHEN CCI IS ACTIVE. BOTH THE ZACTO AND BACTO ARE HIGH WHEN NEITHER CC IS ACTIVE.

INWZD AND INWSD BLOCK INPUT DATA FROM CCO AND CCI WHEN THEY ARE ACTIVE.

LEAD 100D WILL BE ACTIVE WHEN EITHER LOSE OF THE INPUT DATA BIT IS PRESENT. IT CAN BE USED BY AN EXTERNAL CIRCUIT TO INDICATE WHEN INCOMING DATA IS PRESENT. THE EXTERNAL CIRCUIT MUST HAVE SUFFICIENT FILTERING TO HOLD OVER ANY GAP BETWEEN LOSES.

INPUT B0P1 IS USED TO INITIALIZE THE 1211 AND 1212 TO THE 00 STATE, AND TO CLEAR THE ACT FLIP-FLOP. THIS SIGNAL MAY BE ACTIVATED BY AN EXTERNAL CIRCUIT AT THE END OF A DATA COMMUNICATION.

LOGIC LEVEL TO BIPOLAR CONVERSION

THE 3A CC FOLLOWS THE DATA PORTION OF A COMMUNICATION TO A PERIPHERAL UNIT WITHIN AN ALL-ZEROS BIT STREAM. THIS BIT STREAM IS USED BY THE PERIPHERAL UNIT AS BIT TIMING FOR THE BIPOLAR DATA SET BY THE 3A CC. THE 3A CC MAINTAINS THE ZEROES BIT STREAM UNTIL IT RECEIVES A REPLY FROM THE PERIPHERAL UNIT, OR UNTIL THE NEXT BIT PERIOD. IN WHICH IT SHOULD RECEIVE A REPLY IS EXCEEDED. THUS, FOR EACH OUTGOING BIT PERIOD, LEAD A1 (OR C1) IS ACTIVE FOLLOWED BY B1 (OR D1) ACTIVE. INPUTS EN0B AND EN0D ARE ACTIVATED TO START THE OUTPUT AND DIRECT IT TO CCO OR CCI.

GATES 211W, 220 AND 212, 200 ARE TRANSFORMER-COUPLED TO THE OUTGOING DATA LINE TO CCO. GATES 0110, 220 AND 012, 200 ARE TRANSFORMER-COUPLED TO THE OUTGOING DATA LINE TO CCI. THESE GATES ARE HELD HIGH DURING THERE IS NO INCOMING DATA OR WHEN THE ENABLE LEAD (EN0B, EN0D) IS NOT ACTIVE.

THE RELATIONSHIP BETWEEN THE ALL-ZEROS INPUT DATA, THE LOGIC LEVEL OUTGOING DATA LEAD, AND THE BIPOLAR OUTPUT DATA IS SHOWN IN FIG. 2. THE LOGIC LEVEL OUTGOING DATA SIGNAL (000) IS TROGLED INTO PRIOR TO THE BIT PERIOD. THE OUTPUT OF 000 IS COMBINED WITH THE TIMING SIGNALS DERIVED FROM THE INCOMING DATA (TC1210 AND TC1220) TO DETERMINE THE ORDER IN WHICH 211W, 220 AND 212, 200 WILL BE ACTIVE. IF A ONE IS SET, TC1210, 221 WILL BE ACTIVE DURING THE FIRST LOSE AND TC1212, 201 WILL BE ACTIVE DURING THE SECOND LOSE. THE REVERSE WILL BE TRUE TO OUTPUT A ZERO. THESE SIGNALS WILL BE INVERTED BY THE ENABLED OUTPUT GATES 2110, 220 AND 212, 200 AND/OR 011, 220 AND 012, 200.

A GATE IN EACH PAIR IS CONNECTED TO THE OPPOSITE END OF THE PRIMARY OF A TRANSFORMER. EACH PAIR OF GATES IS PROVIDED WITH A TRANSFORMER. THUS, THE ORDER IN WHICH THE GATES ARE ACTIVE DETERMINES THE POLARITY OF THE PULSE AVAILABLE AT THE TRANSFORMER SECONDARY.

NOTE THAT THE 100 AND 101 ARE TROGLED INTO CCO OR B0C (OR D0C) DURING THE BIT INTERVAL PRECEDING THAT IN WHICH THE BIT IS TROGLED INTO THE INPUTS S0B0 AND P0B0 ALIGNED DIRECT SEED AND CLEAR OPERATIONS ON B0B.

SIGNAL LEAD

C. MECHANICS

JUNCTIONS

ACTP

ACTO

A1

B0C

C1

D0C

EN0B

EN0D

100

101

1211

1212

1220

B0B

B0C

B1

B2

B3

B4

B5

B6

B7

B8

B9

B10

B11

B12

B13

B14

B15

B16

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